Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III EXAMINATION – SUMMER 2016

Subject Code:130704 Date:27/05/2016

Subject Name:Computer Organization and Architecture

Time:10:30 AM to 01:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain the Common Bus System with its diagram.	**07**
	(b)	Explain Organization of Memory Stack with related operations.	**07**
Q.2	**(a)**	Explain BCD adder with block diagram.	**07**
	(b)	Explain the Instruction Cycle with flowchart.	**07**
		OR	
	(b)	List out the Characteristics of CISC and RISC.	**07**
Q.3	**(a)**	Explain different types of Shift Micro operations.	**07**
	(b)	Explain Design of Control Unit.	**07**
		OR	
Q.3	**(a)**	Explain input-output instructions.	**07**
	(b)	Discuss following Instructions. i) SZA ii) LDA iii) ISZ iv) CIR v) CIL vi) SZE vii) BSA	**07**
Q.4	**(a)**	Explain the Instruction Pipelining with Example.	**07**
	(b)	Explain the Working of Second Pass Assembler with its flowchart.	**07**
		OR	
Q.4	**(a)**	Explain First Pass Assembler.	**07**
	(b)	Explain the booth's Algorithm with the help of flowchart.	**07**
Q.5	**(a)**	What is addressing mode? List and Explain any two addressing mode.	**07**
	(b)	Explain Address Sequencing with block diagram.	**07**
		OR	
Q.5	**(a)**	What is Array Processor? Explain SIMD Array Processor.	**07**
	(b)	Explain Memory-Reference Instructions with flowchart.	**07**

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