Seat No.: \_\_\_\_\_

Enrolment No.\_\_\_\_

## **GUJARAT TECHNOLOGICAL UNIVERSITY**

BE - SEMESTER- III(OLD) EXAMIN	NATION – SUMMER 2019
Subject Code: 130704	Date: 18/06/2019
<b>Subject Name: Computer Organization Ar</b>	nd Architecture
Time: 02:30 PM TO 05:00 PM	Total Marks: 70
Instructions:	
1. Attempt all questions.	

- Attempt an questions.
   Make suitable assumptions wherever necessary.
- 3. Figures to the right indicate full marks.

Q.1	(a) (b)	Explain the Common Bus System with its diagram. Explain the register transfer language with example.	07 07
Q.2	(a) (b)	List and explain different types of shift micro operation. Explain Instruction cycle.	07 07
	<b>(b)</b>	OR Explain register stack and memory stack with block diagram.	07
Q.3	(a) (b)	Explain the different addressing modes with suitable examples.  Explain different types of Interrupts.	07 07
Q.3	(a) (b)	OR  Explain the design of Accumulator logic.  Draw and explain the organization of micro programmed control unit.	07 07
Q.4	(a) (b)	Explain address sequencing with block diagram. Give the detailed comparison between RISC and CISC.	07 07
Q.4	(a) (b)	OR Explain an Address Symbol Table with a suitable example. What is an array processor? Explain the different types of array Processor.	07 07
Q.5	(a) (b)	Explain the Instruction Pipelining with example.  Explain the Booth Multiplication Algorithm in detail.	07 07
0.5	(a)	OR Explain the first pass of an assembler with a flowchart.	07

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(b) Explain the BCD adder and its working with block diagram.

**07**