Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III • EXAMINATION – WINTER • 2014

Subject Code: 130704 Date: 18-12-2014

Subject Name: Computer Organization and Architecture

Time: 02.30 pm - 05.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	What is an Interrupt Cycle? Draw and explain flow chart of it.	**07**
	(b)	What is an Assembler? Explain its passes in detail.	**07**
Q.2	**(a)**	Explain the control gate structure for the Address Register in a basic computer system.	**07**
	(b)	List different addressing modes. Explain any one in details.	**07**
		OR	
	(b)	What is a memory stack? Explain clearly with example.	**07**
Q.3	**(a)**	Explain MRI and Non-MRI with example.	**07**
	(b)	Write an ALP to multiply TWO numbers using successive addition method	**07**
		OR	
Q.3	**(a)**	List the characteristics of RISC architecture.	**07**
	(b)	Write an ALP to transfer a block of 10 bytes from one location to other.	**07**
Q.4	**(a)**	What is pipeline processing? Explain its significance with respect to the processor architecture.	**07**
	(b)	Describe the importance of timing and control signal in data transfer with example.	**07**
		OR	
Q.4	**(a)**	Explain Booth algorithm for multiplication operation.	**07**
	(b)	Draw the block diagram for BCD adder and explain it.	**07**
Q.5		Attempt **ANY FOUR**	**14**
	(a)	Register Transfer Language	
	(b)	Vector Processing	
	(c)	Machine Language	
	(d)	Shift Micro-operations	
	(e)	Parallel Processing	
	(f)	Push and Pop operation on register stack	

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