Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III EXAMINATION – WINTER 2015

Subject Code:130704 Date:18/12/2015

Subject Name: Computer Organization and Architecture

Time: 2:30pm to 5:00pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain 4-bit Binary Adder - Subtractor with diagram.	**07**
	(b)	Explain construction of common bus system with three-state buffers using diagram.	**07**
Q.2	**(a)**	Explain different phases of an instruction cycle with flowchart.	**07**
	(b)	Explain hardwired control unit of basic computer with diagram.	**07**
		OR	
	(b)	Give instruction code format of memory reference instructions. List and explain memory reference instructions in brief.	**07**
Q.3	**(a)**	Answer the following.	
		1. What is pseudo instruction? List pseudo instructions of basic computer with importance of each.	**03**
		2. Address symbol table.	**02**
		3. Subroutine and data linkage.	**02**
	(b)	Explain Micro program sequencer for a control memory with diagram.	**07**
		OR	
Q.3	**(a)**	Draw flowchart for second pass of assembler and explain it briefly.	**07**
	(b)	Answer the following.	
		1. Mapping from instruction code to microinstruction address.	**04**
		2. Microinstruction code format.	**03**
Q.4	**(a)**	Explain organization of memory stack with related operations.	**07**
	(b)	Explain different types of addressing modes.	**07**
		OR	
Q.4	**(a)**	Explain 4-bit status register. Draw block diagram of an 8-bit ALU with 4-bit status register.	**07**
	(b)	Explain Four-segment instruction pipeline with diagram.	**07**
Q.5	**(a)**	Explain pipeline conflicts.	**07**
	(b)	Explain BCD adder with block diagram.	**07**
		OR	
Q.5	**(a)**	Draw flowchart for add and subtract operations with signed magnitude data. Explain it briefly.	**07**
	(b)	Explain Booth multiplication algorithm with flowchart.	**07**

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