

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER-III (OLD) EXAMINATION – WINTER 2018

Subject Code:130704

Date:10/12/2018

Subject Name:Computer Organization And Architecture

Time:10:30 AM TO 01:00 PM

Total Marks: 70

Instructions:

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1** (a) Explain Register reference and memory reference instructions in detail. **07**
(b) Explain 4-bit Binary Adder - Subtractor with diagram. **07**

- Q.2** (a) Explain the common bus system with its diagram. **07**
(b) Explain the difference between hard wired control and micro programmed control. **07**

OR

- (b) Explain the Instruction Cycle with flowchart. **07**

- Q.3** (a) What is the basic functionality of an assembler? Draw and explain its first pass. **07**
(b) Explain four-segment instruction pipeline with diagram. **07**

OR

- Q.3** (a) Write ALP to add two double precision numbers. **07**
(b) List out the Characteristics of CISC and RISC. **07**

- Q.4** (a) Explain four-segment instruction pipeline with diagram **07**
(b) What is addressing mode? Explain different types of addressing modes. **07**

OR

- Q.4** (a) What is a register stack? Explain PUSH and POP operations on it. **07**
(b) Draw and explain the organization of microprogrammed control unit. **07**

- Q.5** (a) Explain the Booth's algorithm with flowchart. **07**
(b) Explain BCD adder with block diagram. **07**

OR

- Q.5** (a) What is Array Processor? Explain SIMD Array Processor. **07**
(b) What is vector processing? What is the use of vector processing? **07**
