

GUJARAT TECHNOLOGICAL UNIVERSITY
BE - SEMESTER-III (NEW) • EXAMINATION – SUMMER 2015

Subject Code: 2131004

Date: 27/05/2015

Subject Name: DIGITAL ELECTRONICS

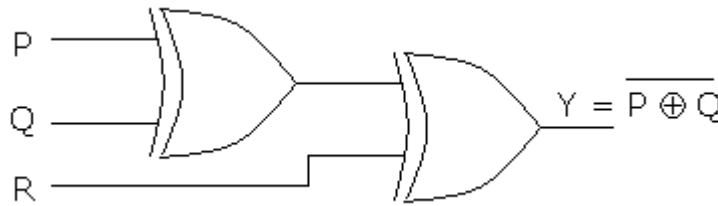
Time: 02.30pm-05.00pm

Total Marks: 70

Instructions:

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1 (a)** Do as directed **07**
- (i) Convert $(75)_{10} = (\text{_____})_2$ **01**
- (ii) Convert $(101011)_2 = (\text{_____})_{10}$ **01**
- (iii) Convert $(10101101)_2 = (\text{_____})_{16} = (\text{_____})_8$ **02**
- (iv) What is self complementing code? Represent $(472)_{10}$ in 2421 self complementing code. **02**
- (v) Find the logic required at R input. **01**



- (b) (i) Convert $(96)_{10}$ to its equivalent gray code and EX-3 code. **04**
- (ii) Perform addition in BCD format $(79)_{BCD} + (16)_{BCD}$ **03**
- Q.2 (a)** Reduce the given function using K-map and implement the same using gates. **07**
- $F(A,B,C,D) = \sum m(0,1,3,7,11,15) + \sum d(2,4)$
- (b) Design a circuit for 2-bit magnitude comparator. **07**

OR

- (b) Design 3-bit even parity generator circuit. **07**
- Q.3 (a)** (i) State De Morgan's theorems and prove with the help of truth table. **04**
- (ii) Convert $F(A, B, C) = BC + A$ into standard minterm form. **03**
- (b) Draw the truth table of full adder and implement using minimum number of logic gates. **07**

OR

- Q.3 (a)** (i) Discuss NAND gate as universal gate (implement NOT, AND, OR & NOR gate using NAND gate). **04**
- (ii) Perform subtraction of $(78)_{10} - (58)_{10}$ using 2's complement method. **03**
- (b) Draw the truth table of full subtractor and implement using minimum number of logic gates. **07**

- Q.4 (a)** Design 4 X 16 decoder using two 3 X 8 decoder. **07**
- (b) Convert D flip flop into SR flip flop **07**

OR

- Q.4 (a)** Implement the given function using 8 X 1 Multiplexer **07**
 $F(A,B,C,D) = \sum m(0,1,2,3,5,8,9,11,14)$
- (b)** With the help of function table and circuit diagram explain the working of clocked SR flip flop. **07**
- Q.5 (a)** Design 4-bit ripple counter using negative edge triggered JK flip flop. **07**
- (b)** Compare ROM, PLA and PAL **07**

OR

- Q.5 (a)** With neat sketch design 4-bit bidirectional shift register. **07**
- (b)** Define followings (i to iv with respect to logic families and v to vii with respect to finite state machine) **07**
- (i) Fan in
 - (ii) Fan out
 - (iii) Noise Margin
 - (iv) Propagation delay
 - (v) State table
 - (vi) Melay machine
 - (vii) Moore machine
