Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III • EXAMINATION – SUMMER • 2014

Subject Code: 130701 Date: 26-05-2014

Subject Name: Digital Logic Design

Time: 02.30 pm - 05.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Covert following 1. $(4E7.2)_{16} = (?)_8$ 2. $(521.3)_8 = (?)_2$ [	**06**
	(b)	Simplify : 1. A'B + A'BC' + A'BCD + A'BC'D'E 2. (P+Q+R) (P' + Q' + R') P	**08**
Q.2	**(a)**	Write a brief not on Gray codes. Also discuss methods for conversion from gray to binary code and vice versa	**07**
	(b)	Using K-map find the Boolean function and its complement for the following: $F(A,B,C,D) = \sum(1,2,3,4,6,8,9,10,11,12,14)$	**07**
		OR	
	(b)	Derive Boolean function using Tabulation Method for the following: $F(P,Q,R,S) = \sum(0,1,3,4,5,7,10,13,14,15)$	**07**
Q.3	**(a)**	Explain in brief: Programmable Logic Array	**07**
	(b)	Attempt following: 1. Covert into Sum-of-Minterms : A' + B + CA 2. Covert into Product-of-Maxtems : A(A'+B)(C')	**07**
		OR	
Q.3	**(a)**	Write a brief note on edge-triggered SR and JK Flip-Flops.	**07**
	(b)	Prove that: 1. ((AB'+ABC)' + A(B+AB'))' = 0 2. AB'C + A'BC + ABC = AC + AB	
Q.4	**(a)**	Design a sequential circuit using JK Flip-Flops and two states Q0 and Q1 such that , 1. It moves to the next state for input 0. (00 to 01, 01 to 10,…, 11 to 00) 2. It moves to the previous state for input 1. (reverse from the above mentioned steps)	**09**
	(b)	Write a brief note on parity checker/generator.	**05**
		OR	
Q.4	**(a)**	Design and Implement a Mod-10 asynchronous counter with T FF.	**07**
	(b)	Design a circuit for 4-bits parallel register with load with D Flip-Flops. Load input decides whether to load new input or to apply no change conditions.	**07**
Q.5	**(a)**	Discuss hard-wired vs. micro-programmed control unit.	**07**
	(b)	Write a note on Binary Ripple Counter.	**07**
		OR	
Q.5	**(a)**	Write a note on Master-Slave Flip-Flop.	**07**
	(b)	Design a 4-to-16 decoder by using only 2-4 decoder circuits	**07**

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