

GUJARAT TECHNOLOGICAL UNIVERSITY
BE - SEMESTER- III EXAMINATION – SUMMER 2015

Subject Code:130701

Date:04/06/2015

Subject Name: Digital Logic Design

Time: 02.30pm-05.00pm

Total Marks: 70

Instructions:

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1 (a)** Convert following numbers. **07**
(a) $(4021.2)_5 = ()_{10}$. (b) $(B65F)_{16} = ()_{10}$. (c) $(630.4)_8 = ()_{10}$. (d) $(41)_{10} = ()_2$.
- (b)** Using 10's complement, subtract : $(72532-3250)_{10}$ **07**
Using 10's complement, subtract : $(3250-72532)_{10}$
Using 2's complement, subtract : $(1010100-1000100)_2$
- Q.2 (a)** Explain error detection codes and the reflected code with examples. **07**
(b) Express the Boolean function $F=A+B'C$ a sum of minterms and in sum of max terms. **07**
- OR**
- (b)** Draw and explain two input (i) AND (ii) OR and (iii) EX-OR gates. **07**
- Q.3 (a)** Define and explain (i) fan out (ii) power dissipation and (iii) Propagation delay. **07**
(b) Simplify the Boolean function $F(x,y,z) = \sum(0,2,4,5,6)$ using K- map. Explain groups. **07**
- OR**
- Q.3 (a)** Explain wired logic with examples. **07**
(b) Design half adders and explain various implementations. **07**
- Q.4 (a)** Explain design and functioning of half and full subtractors. **07**
(b) Design BCD to excess-3 code converter. **07**
- OR**
- Q.4 (a)** Design converter to convert decimal 8,4,-2,-1 code to BCD. **07**
(b) Design converter to convert decimal code 2,4,2,1 to 8,4,-2,-1 code. **07**
- Q.5 (a)** Design a BCD adder. **07**
(b) Explain 3 to 8 line decoder. **07**
- OR**
- Q.5 (a)** Explain ROM and it's types. **07**
(b) Explain PLA and it's application. **07**
