Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (OLD) - EXAMINATION – SUMMER 2017

Subject Code: 130701 **Date: 31/05/2017**

Subject Name: Digital Logic Design

Time: 10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	(a)	Convert $4BAC_{16}=(\ )_8=(\ )_4=(\ )_2=(\ )_{10}$. Show all steps of conversion.	07
	(b)	Design a circuit for binary to gray conversion. Give Example.	07
Q.2	(a)	Design a full adder circuit using two half adders and gates.	07
	(b)	Describe the block diagram of a Decoder circuit. Implement a 3 to 8 decoder circuit.	07
		OR	
	(b)	Use Tabulation method & solve $\sum m(0,2,6,8)+d(12,13,14,15)$	07
Q.3	(a)	Define SoP expressions. How do they differ from PoS?	07
	(b)	Explain the working of a master slave JK Flip flop.	07
		OR	
Q.3	(a)	Explain the working of a D FF and a T FF using truth table.	07
	(b)	Use Kmap & solve $\sum m(0,2,6,8)+d(12,13,14,15)$. Write answer in SoP and PoS forms.	07
Q.4	(a)	Explain a 4 bit ripple counter using timing diagrams.	07
	(b)	Design a synchronous counter that goes 0,2,3,7,0,2,3,.....	07
		OR	
Q.4	(a)	Explain the working of a BCD ripple counter.	07
Q.4	(b)	Explain the working of a BCD synchronous counter.	07
Q.5	(a)	Explain Macro operation Vs micro operations	07
	(b)	Classify Registers. Describe any one of them in details.	07
		OR	
Q.5	(a)	Explain Processor units. Differentiate ROM and PLA units.	07
	(b)	Compare hard wired control to micro program control devices.	07

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