GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER-III EXAMINATION - WINTER 2015

Subject Code:130701 Date:29/12/2015 Subject Name: Digital logic design Time: 2:30pm to 5:00pm **Total Marks: 70 Instructions:** 1. Attempt all questions. 2. Make suitable assumptions wherever necessary. 3. Figures to the right indicate full marks. 0.1 Convert the following Hexadecimal numbers to Octal 06 (a) 4F7.A8 (b) BC70.OE (c) 42FD **(b)** Prove that 08 (i) $A[B+C(\overline{AB+AC})] = AB$ (ii) $A\overline{B}$ (C+BD) + \overline{A} \overline{B} = \overline{B} C **Q.2** Minimize the following multiple output functions using K-07 Map (i) $F1 = \sum m = (0,2,6,10,11,12,13) + d(3,4,5,14,15)$ (ii) $F2 = \pi M(0,4,9,10,11,14,15)$ Describe briefly TTL fanin, fanout & noise margin with **07** suitable sketches (b) Design a combinational circuit whose input is a four bit 07 number & whose output is the 2's complement of the input number (a) Draw the logic diagrams of NAND & NOR gates & 07 0.3 explain why they are called as universal gates (b) Explain error detecting & correcting codes with the help of 07 a suitable example. OR (a) Explain excess -3 code & gray code **07** Q.3 (b) State & explain Demorgan's theorem **07** 07 **Q.4** (a) Convert the following to other canonical form (i) $F(x,y,z) = \sum (1,3,7)$ (ii) F(A,B,C,D) = π (0,1,2,3,4,6,12)

(b) Implement combinational logic using 8:1line MUX for $F(A,B,C,D) = \sum m(0.2,4,5,7,9,12,15)$

OR

- Q.4 (a) Draw & explain the operation of 4 bit binary parallel adder 07
 Q.4 (b) Draw the logic diagram of 3 to 8 line decoder. Explain 07 its operation with truth table
- Q.5 (a) State & explain any four operating characteristics of a flip 07 flop
 - **(b)** Draw the state diagram & state table for Moore type **07** sequence detector to detect the sequence 110

OR

- Q.5 (a) Explain arithmetic micro operations with the help of a 07 block diagram
 - (b) Discuss the differences between hard wired control & 07 micro program control. State the merits of one over the other
