

Seat No.: _____

Enrolment No. _____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER-IV (NEW) - EXAMINATION – SUMMER 2018

Subject Code:2140707

Date:24/05/2018

Subject Name:Computer Organization

Time:10:30 AM to 01:00 PM

Total Marks: 70

Instructions:

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

		MARKS
Q.1	(a) How negative integer number represented in memory? Explain with suitable example.	03
	(b) Explain floating point representation.	04
	(c) Explain shift micro operations and Draw neat and clean diagram for 4-bit combinational circuit shifter.	07
Q.2	(a) Explain 1) LDA 2) STA 3) ISZ instructions.	03
	(b) Explain DMA operation.	04
	(c) Draw block diagram of Control unit of basic computer and explain it.	07
	OR	
	(c) What is instruction cycle? Draw Flowchart for Instruction cycle and explain it.	07
Q.3	(a) List out types of interrupt. Explain any one.	03
	(b) List out address sequencing capabilities required in control memory.	04
	(c) Explain instruction format with example.	07
	OR	
Q.3	(a) Write short note on RISC .	03
	(b) Differentiate hardwired control and micro programmed control architecture.	04
	(c) List out addressing mode of instructions and explain with example.	07
Q.4	(a) What is cache coherence?	03
	(b) Explain pipeline processing conflict.	04
	(c) Explain Flynn's classification.	07
	OR	
Q.4	(a) What is cache miss and cache hit?	03
	(b) Explain the significance of every bit of Program Status Word (PSW).	04
	(c) What is speedup? Derive the equation of speedup for k-segment pipeline processing for task.	07
Q.5	(a) State the differences between register stack and memory stack.	03
	(b) Differentiate isolated I/O and memory mapped I/O.	04
	(c) Draw flowchart hardware multiplication algorithm and explain it.	07
	OR	
Q.5	(a) What is tightly coupled and loosely coupled multiprocessor architecture.	03
	(b) Differentiate Programmed I/O and Interrupt initiated I/O	04
	(c) Draw and explain shared memory architecture of multiprocessor system.	07
