

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER-IV (NEW) EXAMINATION – WINTER 2018

Subject Code:2140707

Date:05/12/2018

Subject Name:Computer Organization

Time: 02:30 PM TO 05:00 PM

Total Marks: 70

Instructions:

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

		MARKS
Q.1	(a) Represent $(8620)_{10}$ in (1) binary (2) Excess-3 code and (3) 2421 code.	03
	(b) Explain 4-bit adder-subtractor with diagram.	04
	(c) Explain four types of instruction formats.	07
Q.2	(a) Explain selective set, selective complement and selective clear.	03
	(b) Explain error detection with odd parity bit.	04
	(c) Draw the block diagram of 4-bit arithmetic circuit and explain it in detail.	07
	OR	
	(c) Explain flow chart of Interrupt Cycle with diagram.	07
Q.3	(a) Explain logical shift, circular shift and arithmetic shift micro operations.	03
	(b) Explain following instructions: (1) AND (2) BUN (3) STA (4) ISZ	04
	(c) What is register stack? Explain push and pop micro-operations.	07
	OR	
Q.3	(a) Explain Three-state bus buffer.	03
	(b) Explain Direct and Indirect Addressing.	04
	(c) Explain second pass of an assembler with diagram.	07
Q.4	(a) Write brief note on subroutine call and return	03
	(b) Draw space-time diagram for 4-segment pipeline with 8 tasks.	04
	(c) Write an assembly program to multiply two positive numbers.	07
	OR	
Q.4	(a) Write brief note on RISC.	03
	(b) Explain Booth Multiplication Algorithm.	04
	(c) Write an assembly program to add 10 numbers from memory.	07
Q.5	(a) Describe SIMD array processor.	03
	(b) Explain BCD adder in brief.	04
	(c) How main memory is useful in computer system? Explain the memory address map of RAM and ROM.	07
	OR	
Q.5	(a) Describe the followings : 1) Data dependency 2) Pseudo instruction 3) Effective address	03
	(b) Explain Daisy chain priority interrupt.	04
	(c) Discuss associative mapping and direct mapping in organization of cache memory.	07
