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# GUJARAT TECHNOLOGICAL UNIVERSITY

**BE - SEMESTER–V • EXAMINATION – WINTER • 2014**

**Subject Code: 150701** **Date: 26-11-2014**

**Subject Name: Advanced Processors**

**Time: 10.30 am - 01.00 pm** **Total Marks: 70**

**Instructions:**

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

| | | | |
|---|---|---|---|
| Q.1 | (a) | Draw and explain the 8086 microprocessor architecture. | 07 |
| | (b) | Explain the concept of segmented memory? What are its advantages? | 07 |
| Q.2 | (a) | 1) Differentiate between microprocessor and microcontroller.<br>2) What is an instruction queue? Explain in details. | 07 |
| | (b) | Explain the following instructions:<br>1) LDS 2) PUSHF 3) DAA 4) CBW 5) SAR 6) RCR 7) RET | 07 |
| | | **OR** | |
| | (b) | 1) The original contents of AX, BL, word-sized memory location SUM, and carry flag CF are 1234H, ABH, 00CDH, and 0H, respectively. Describe the results of executing the following sequence of instructions:<br>ADD AX, [SUM]<br>ADC BL, 05H<br>INC WORD PTR [SUM]<br>2) Compare the minimum and maximum modes of the 8086 microprocessor. | 04<br>03 |
| Q.3 | (a) | Write an 8086 assembly program to find largest of two 8-bit numbers. | 07 |
| | (b) | Explain different types of registers in 8086 microprocessor architecture. | 07 |
| | | **OR** | |
| Q.3 | (a) | Write an 8086 assembly program to sum of series of 8-bit numbers. | 07 |
| | (b) | Explain the flag register format of 80286 with suitable figure. | 07 |
| Q.4 | (a) | Draw and explain the internal block diagram of 80286 microprocessor. | 07 |
| | (b) | Explain the 80386 microprocessor register set. | 07 |
| | | **OR** | |
| Q.4 | (a) | Draw and explain the internal block diagram of 80486 microprocessor. | 07 |
| | (b) | Explain the addressing modes of 80386 with examples. | 07 |
| Q.5 | (a) | Explain the MMX and Hyper Threading. | 07 |
| | (b) | What is descriptor table? What is its use? Dedifferentiate between GDT and LDT. | 07 |
| | | **OR** | |
| Q.5 | (a) | Give and explain the architecture of SUN SPARC processor. | 07 |
| | (b) | Differentiate the RISC architecture and CISC architecture. | 07 |

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