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GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER-V (NEW) - EXAMINATION - SUMMER 2016 Subject Code:2150907 Date:06/05/2016

Subject Name:Microprocessor and Microcontroller Architechture & Interfacing

Time:02:30 PM to 05:00 PM Total Marks: 70

Instructions:

- 1. Attempt all questions.
- 2. Make suitable assumptions wherever necessary.
- 3. Figures to the right indicate full marks.
- Q.1 (a) Discuss the internal RAM structure of 8051. Explain SFR space in detail. 07
 - **(b)** What are the addressing modes for 8051? Explain in brief giving suitable **07** example.
- Q.2 (a) Explain the function of following pins in 8085. OD, HLDA, READY & TRAP.
 - (b) Explain the programming model of 8085. State the purpose of temporary register W & Z.

OR

- (b) Draw & explain the physical port structure and also list the alternate functions of all the ports of 8051.
- Q.3 (a) Write a 'C' program to find average of 10 numbers stored in external memory & store the result in register R2.
 - (b) With the help of diagram show how de-multiplexing of address/data lines AD0- $\overline{AD7}$ can be achieved? Also explain the generation of control signals \overline{MEMW} , \overline{MEMR} , IOR & IOW.

OR

- Q.3 (a) Write a 'C' program to generate a square wave of frequency 10 KHz on P1.2 07
 - **(b)** Explain all the bits of TMOD register & hence find the control word for selecting timer 0 in mode 2.
- Q.4 (a) Explain the special function registers SCON & SBUF in 8051 serial 07 communication.
 - (b) Write an assembly program to add two 16 bit numbers. 07

OR

- Q.4 (a) What are the interrupts available in 8051? What is the default priority & how it can be changed?
 - (b) Why C programming is preferred to assembly programming? What are the data types available in C?
- Q.5 (a) With the help of diagram explain the interfacing of seven segment display with 07 8051.
 - (b) Differentiate between SJMP & LJMP, RET & RETI, MOVX & MOVC. 07

- Q.5 (a) Write a short note on different types of memory.
 (b) Compare Von-Neumann & Harvard architecture, CISC & RISC processors.
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