Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VI (NEW) - EXAMINATION – SUMMER 2018

Subject Code: 2160909 **Date: 08/05/2018**

Subject Name: Advance Microcontrollers

Time: 10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Compare Von Neumann and Harvard architecture.	**03**
	(b)	Discuss about enumerator.	**04**
	(c)	Interface 8051 to external ROM and RAM and explain how 8051 access them?	**07**
Q.2	**(a)**	List the advantages of Thumb-2 instruction set technology.	**03**
	(b)	Write features of STM32F4xx.	**04**
	(c)	Discuss about the concept of SPI and I2C communication protocols for microcontrollers.	**07**
		OR	
	(c)	Draw and explain block diagram of MPC 3304(ADC).	**07**
Q.3	**(a)**	Why the watchdog timer is necessary for any embedded system? Give its reasons.	**03**
	(b)	Give the significance of C compiler, Debugger, Assembler and Flash programmer.	**04**
	(c)	Explain Bit-Banding technique with suitable example.	**07**
		OR	
Q.3	**(a)**	Differentiate ISP (In System Programming) and IAP (In Application Programming).	**03**
	(b)	Explain multi-AHB bus matrix in STM32F4xx.	**04**
	(c)	What do you mean by pipelining? Explain 3-stage pipelining architecture in Cortex CPU.	**07**
Q.4	**(a)**	Explain the sources of STM32 system reset.	**03**
	(b)	Enlist features of P89V51RD2.	**04**
	(c)	Which are the different modes of operation of PCA timer? Explain any one with suitable example.	**07**
		OR	
Q.4	**(a)**	Write a short note on CCON register in PCA timer.	**03**
	(b)	Explain the concept of PUSH and POP operation in the Cortex M processors.	**04**
	(c)	Explain the system architecture of STM32.	**07**
Q.5	**(a)**	Compare CISC and RISC architecture.	**03**
	(b)	Write a note on the programmer's model of The Cortex-M0.	**04**
	(c)	Explain features and functional description of TIM 6 & TIM 7 basic timers.	**07**
		OR	
Q.5	**(a)**	Explain the concept of memory segmentation in Cortex processor.	**03**
	(b)	What do you mean by exceptions? What are the sources of exceptions?	**04**
	(c)	What do you mean by GPIOs. Write features of GPIOs.	**07**

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