BE - SEMESTER-VI (NEW) EXAMINATION – WINTER 2017				
Subject Code: 2160909 Date: 20/1			2017	
Subject Name:Advance Microcontrollers				
Time:02:30 PM TO 05:00PM Total Mark			ks: 70	
Instructi	ions:			
		tempt all questions.		
		ake suitable assumptions wherever necessary. gures to the right indicate full marks.		
Q.1	(a)		03	
	(b)	÷ · ·	04	
	(c)	Which are the different modes of operation of the PCA timer? Explain PWM mode in detail with block diagram.	07	
Q.2	(a)	Explain PCA Module 4 as Watchdog Timer.	03	
	(b)	Compare Von Neumann and Harvard architecture.	04	
	(c)	Explain SPI control and status register and draw the machine cycle of SPI data transfer with $CPHA = 0$.	07	
		OR		
	(c)	Write a program to design PCA module of 89V51RD2 to calculate the width of a detected pulse. The pulse must begin with a rising edge and end with a falling edge on the CEX0 pin.	07	
Q.3	(a)	Explain the CCAPMn Register in PCA timer of P89V51RD2.	03	
	(b)	Explain 3stage pipelining in cortex CPU.	04	
	(c)	Write and explain features of STM32F4xx. OR	07	
Q.3	(a)	Explain CCON – PCA register.	03	
	(b)	List out steps required to enable interrupts safely in an IRQ handler.	04	
	(c)	Explain bit banding technique with suitable example.	07	
Q.4	(a)	Explain Round Robin with Interrupt Architecture.	03	
	(b)	•	04	
	(c)	Explain Thumb 2 Instruction set of ARM CORTEX. OR	07	
Q.4	(a)	Explain high speed output toggle mode of 8051 microcontroller.	03	
	(b)	Explain multi-AHB bus matrix in STM32F4XX.	04	
	(c)	Explain the features of GPIO in detail.	07	
Q.5	(a)	What do you mean by enumerator?	03	
	(b)	Explain Round Robin Architecture.	04	
	(c)	Explain GPIO registers in detail.	07	

(a) Explain tail chaining in cortex M processors.

(b) Explain TIM6 timer.(c) Explain NVIC Controller of ARM CORTEX.

Q.5

03

04 **07**