

Seat No.: _____

Enrolment No. _____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER-VI (NEW) - EXAMINATION – SUMMER 2018

Subject Code:2160709

Date:08/05/2018

Subject Name:Embedded & VLSI Design

Time:10:30 AM to 01:00 PM

Total Marks: 70

Instructions:

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1**
- (a) Classify Embedded system along with their applications. **03**
 - (b) Explain depletion region for MOS system under external bias. **04**
 - (c) What is EDLC? Explain different phases of Embedded product Development life cycle. **07**
- Q.2**
- (a) Classify Embedded system memories. **03**
 - (b) Explain watch dog timer and real time clock in brief. **04**
 - (c) Explain the fundamental issues of hardware software co-design in brief. **07**
- OR**
- Q.3**
- (c) Explain VLSI design flow using Y chart. **07**
 - (a) What do you mean by sensors and actuators? **03**
 - (b) Explain the concept of regularity and modularity in brief. **04**
 - (c) Explain fabrication steps of nMOS transistor in detail with necessary diagrams. **07**
- OR**
- Q.3**
- (a) What do you mean by RISC processor? Explain in brief. **03**
 - (b) Explain semicustom design style in brief. **04**
 - (c) Explain operation of MOS transistor with different operation modes in detail **07**
- Q.4**
- (a) Explain the operation of two input depletion load NOR gate. **03**
 - (b) Explain CMOS inverter operation in brief. **04**
 - (c) Explain resistive load inverter and derive its critical voltage points **07**
- OR**
- Q.4**
- (a) Explain controllability and observability. **03**
 - (b) Explain CMOS D-latch in brief. **04**
 - (c) Explain operation of CMOS transmission gates (TGs) in detail. **07**
- Q.5**
- (a) What is UML (unified modeling language). Explain in brief. **03**
 - (b) Explain on chip clock generation and distribution in brief. **04**
 - (c) What is the need for voltage bootstrapping? Explain dynamic voltage bootstrapping circuit with necessary mathematical analysis. **07**
- OR**
- Q.5**
- (a) What is significance of threshold voltage in MOS transistor? Write expression of threshold voltage. **03**
 - (b) Explain Ad Hoc testable design techniques in very brief. **04**
 - (c) Explain NAND gate using CMOS realization, pass transistor and Complementary pass transistor realization. **07**
