Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VI (NEW) EXAMINATION – WINTER 2017

Subject Code: 2160709 Date: 20/11/2017

Subject Name:Embedded & VLSI Design

Time:02:30 PM TO 05:00PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain VLSI Design flow using Y-chart.	**03**
	(b)	Explain various types of Embedded system memories.	**04**
	(c)	Classify Embedded systems along with relevant examples.	**07**
Q.2	**(a)**	Discuss major application areas of an Embedded Systems.	**03**
	(b)	Differentiate: 1. Microprocessor v/s Microcontroller 2. RISC v/s CISC	**04**
	(c)	Derive equation of V_{IL} and V_{IH} for n-type MOSFET inverter with depletion type load.	**07**
		OR	
	(c)	Write a short note on Unified Modeling Language (UML).	**07**
Q.3	**(a)**	What are the advantages of ion implantation over diffusion?	**03**
	(b)	Write I-V equation of P channel MOSFET for all Regions.	**04**
	(c)	What is EDLC? Explain different phases of Embedded Product Development Life Cycle.	**07**
		OR	
Q.3	**(a)**	Explain switching power dissipation of CMOS inverter in brief.	**03**
	(b)	Calculate the threshold voltage V_{TO} at $V_{SB} = 0$, for a polysilicon gate n-channel MOS transistor, with the following parameters: substrate doping density $N_A = 10^{16}$ cm^{-3}, polysilicon gate doping density $N_D = 2 \times 10^{20}$ cm^{-3}, gate oxide thickness $t_{ox} = 500$ Å, and oxide-interface fixed charge density $N_{ox} = 4 \times 10^{10}$ cm^{-2}.	**04**
	(c)	Write down the steps with neat sketch for fabrication of CMOS.	**07**
Q.4	**(a)**	Define: [1] Etching [2] Threshold Voltage [3] Metallization	**03**
	(b)	Why nMOS is better than pMOS transistor?	**04**
	(c)	Write down the steps with neat sketch for fabrication of nMOS.	**07**
		OR	
Q.4	**(a)**	Explain the concept of MOSFET as a switch.	**03**
	(b)	Write a short note on Built In Self-Test (BIST).	**04**
	(c)	Explain the energy band diagram of MOS structure at surface inversion and derive the expression for the maximum possible depth of the depletion region.	**07**
Q.5	**(a)**	Explain Latch up in brief.	**03**
	(b)	Compare Static and Dynamic CMOS logic circuits.	**04**
	(c)	Implement CMOS SR latch based on NAND gates.	**07**
		OR	
Q.5	**(a)**	Define controllability and observability.	**03**
	(b)	Explain Transmission Gate with example.	**04**
	(c)	Discuss RACE problem in Dynamic logic structure.	**07**

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