

Seat No.: _____

Enrolment No. _____

GUJARAT TECHNOLOGICAL UNIVERSITY
MCA - SEMESTER-I • EXAMINATION – WINTER • 2014

Subject Code: 2610004

Date: 01-01-2015

Subject Name: Fundamentals of Computer Organization

Time: 10:30 am - 01:00 pm

Total Marks: 70

Instructions:

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1**
- (a) i) Define the following terms: register, multiplexer, latch 03
ii) Data bits (1011) make a Even Parity Hamming Code 01
iii) 745.81-436.62 (use 9's compliment method) 01
iv) Convert octal number 1762.46 to hexadecimal number 01
v) $1101.11 * 101.1$ 01
- (b) i) State De Morgan's theorem for three variables in both the forms and give the proof for one by the method of perfect induction 03
ii) Reduce the following Boolean expression and draw a logic diagram using AOI logic : 04
 $[(A' + (A+B)')(B' + (B+C)')]'$
- Q.2**
- (a) i) Which are the universal gates? Describe any one. 02
ii) Simplify following Boolean functions using 4 variable K-map 05
1. $F(A,B,C,D) = \sum(3,7,11,13,14,15)$
2. $F(A,B,C,D) = \sum(2,3,5,6,7,9,11,13)$
3. $F(A,B,C,D) = \sum(0,2,8,9,10,11,14,15)$
4. $F(A,B,C,D) = \sum(9,10,12) + d(3,5,6,7,11,13,14,15)$
5. $F(A,B,C,D) = \sum(0,2,4,6,8,10,12,14)$
- (b) Write a short notes on basic components of a digital computers 07
- OR**
- (b) Briefly explain the working of any three peripheral devices. 07
- Q.3**
- (a) Design and explain binary counter to count from 0 to 7 07
(b) 1. Explain full adder using two half adder 04
2. Explain integer representation of binary in digital machines. 03
- OR**
- Q.3**
- (a) Explain shift register with wave form and circuit diagram 07
(b) Explain basic working and application of Multiplexer in detail 07
- Q.4**
- (a) Derive a Boolean expression (in POS form) for a 3 input gating network that will have outputs 0 when all the 3-inputs are same outputs are to be 1 for all other cases. 07
(b) Describe different types of buses. Explain interface of buses with processor, memory and I/O devices 07
- OR**
- Q.4**
- (a) Derive Boolean expression (in SOP form) for a logic circuit that will have a 1 output when $X=0, Y=0, Z=1$ and $X=1, Y=1, Z=0$ and a 0 output for all other input states. 07
(b) What do you mean by Addressing Techniques? Explain Indirect and Indexed Addressing techniques with an example. 07

- Q.5 (a)** Explain working of following instructions with example **07**
1. MOV
 2. XOR
 3. CMP
 4. NEG
 5. AND
 6. OR
 7. MUL
- (b)** Describe two-address and zero-address instruction word formats. **07**
- OR**
- Q.5 (a)** Draw the block diagram of 8086 and explain queue and segment registers. **07**
- (b)** Explain different addressing modes of 8086 with example. **07**
