Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

MCA - SEMESTER–I • EXAMINATION – WINTER - 2017

Subject Code: 3610004 Date: 05-01-2018

Subject Name: Fundamental of Computer Organization

Time: 10:30 am to 01:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	i) What is a BCD code? What are its advantages and disadvantages?	**03**
		ii) Where does complements are used? Compare 1's complement with 2'scomplement.	**03**
		iii) How many different binary numbers can be stored in a register consisting of six switches ?	**01**
	(b)	i) Convert 0.4375 decimal number to equivalent binary number.	**01**
		ii) Convert 111011.1011binary number to equivalent decimal number.	**01**
		iii) 1001.1+1011.01	**01**
		iv) 11.11-10.111 using 2's compliment method	**01**
		v) 1010*101	**01**
		vi) 24.1 – 13.4 using 9's complement method.	**01**
		vii) What is mean by two-state device?	**01**
Q.2	**(a)**	Simplify the following expressions and draw block diagram of the circuit for each simplified expression, using AND and OR gate. i) AB'C' + A'B'C' + A'BC'+A'B'C ii) A(A+B+C) (A'+B+C) (A+B'+C) (A+B+C')	**07**
	(b)	Explain the block diagram of basic components of digital computer.	**07**
		OR	
	(b)	Write note on magnetic disk memories.	**07**
Q.3	**(a)**	(X, Y, Z, W)= Σm (4, 6, 7, 8) + D (2, 5, 11, 12) using K-map 1. Find SOP expression 2. Implement this simplified expression using two level AND-to-OR gate networks. Implement this expression using NAND gates only.	**07**
	(b)	What do you mean by Addressing Techniques? Explain Indirect and Indexed Addressing techniques with an example	**07**
		OR	
Q.3	**(a)**	Derive the Boolean algebra expression for gating network that will have output 0 only when X=1, Y=1, Z=1; X=0, Y=0, Z=0; X=1, Y=0, Z=0. The output is to be 1 for all other cases. 1. Find POS expression 2. Implement this simplified expression using two level OR-to-AND gate network. Implement this expression using NOR gates only.	**07**
	(b)	Explain the Concepts of Address Bus, Data Bus and Control Bus, Bus Width.	**07**
Q.4	**(a)**	Explain shift register with wave form and circuit diagram.	**07**
	(b)	i) Explain full adder using two half adder.	**04**

ii) Explain integer representation of binary in digital machines. **03**

OR

Q.4 **(a)** Design and explain binary counter to count from 0 to 7. **07**

(b) Write working and application of multiplexer. **07**

Q.5 **(a)** Explain various parts of EU in 8086. **07**

(b) How to write assembly code for the instruction C=A+B using zero, one and two addressing technique. **07**

OR

Q.5 **(a)** Draw the block diagram of 8086 and explain queue and segment registers. **07**

(b) i) Draw the truth table of AND and XOR gate. **03**

ii) State De Morgan's theorems. Explain any one **04**

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